

The listing of claims below replaces all prior versions and listings of claims in the application.

**IN THE CLAIMS:**

1. (currently amended) A method of fabricating a field effect transistor (FET) having a metal gate structure, comprising:

forming a structure including a metal gate structure, a source region, and a drain region, said metal gate structure formed in an opening within a dielectric region formerly occupied by a sacrificial gate, said source region and said drain region being disposed on opposite sides of said metal gate structure, and said metal gate structure including:

a first conductive layer including one or more materials selected from the group consisting of metals and compounds of metals, said first conductive layer separated from contacting a gate dielectric, the gate dielectric contacting a transistor channel region ~~formed in a semiconductor region of a substrate~~ by a thickness of a gate dielectric; and

an overlying conductive silicide layer overlying said first conductive layer,

; and

~~forming a source region and a drain region on opposite sides of said metal gate structure.~~

2. (currently amended) The method of claim 1 wherein said step of forming said metal gate structure includes depositing a layer of silicon over said first conductive layer, depositing a layer of metal over said layer of deposited silicon, and reacting said

deposited silicon with said deposited metal to form said overlying silicide layer in a self-aligned manner.

3. (currently amended) The method of claim 2 wherein said step of forming said metal gate structure further includes forming an underlying layer of silicide at an interface between said first conductive layer and said layer of deposited silicon.

4. (currently amended) The method of claim 3 wherein said first conductive layer consists essentially of a single metal whose work function has a value at about the middle bandgap of silicon.

5. (original) The method of claim 4 wherein said single metal is tungsten.

6. (original) The method of claim 5 wherein said underlying layer of silicide consists essentially of tungsten silicide.

7. (original) The method of claim 6 wherein said overlying silicide layer consists essentially of cobalt silicide.

8. (original) The method of claim 6 wherein said overlying layer of silicide consists essentially of nickel silicide.

9. (original) The method of claim 1 wherein said gate dielectric includes a material

selected from the group consisting of silicon dioxide, silicon nitride, silicon oxynitride, hafnium oxide, and zirconium oxide.

10. (original) The method of claim 1 wherein said opening in said dielectric region is lined with dielectric spacers, said dielectric spacers having been formed on sidewalls of said sacrificial gate.

11. (original) The method of claim 10 wherein said dielectric spacers include L-shaped oxide spacers having sidewalls exposed at said opening and overlying nitride spacers.

12. (currently amended) A method of fabricating a field effect transistor (FET), comprising:

forming a source region and a drain region in a semiconductor substrate and a sacrificial gate disposed between a pair of spacers over a overlying said semiconductor region of a substrate, said ;

~~forming a source region and~~ said a drain region being disposed on opposite sides of said sacrificial gate;

forming a dielectric layer on said substrate having a top surface generally planar to a top of said sacrificial gate;

removing said sacrificial gate to form an opening between said pair of spacers, said opening extending to said semiconductor region;

forming a gate dielectric on said semiconductor region in said opening;

forming a first conductive layer in said opening including at least one material

selected from the group consisting of metals and compounds of metals;

depositing a layer of silicon on said first layer in said opening;

removing said dielectric layer and forming a second metal layer including a silicide-forming metal over said source region and said drain region and said layer of silicon; and

annealing said substrate to form a silicide from said silicide-forming metal, said silicide contacting said source region and said drain region and contacting said layer of silicon.

13. (currently amended) The method of claim 12 wherein said annealing also forms a silicide at an interface between said first ~~metal~~conductive layer and said layer of silicon.

14. (original) The method of claim 13 wherein said silicide-forming metal includes at least one metal selected from the group consisting of cobalt, nickel, titanium and platinum.

15-20. (cancelled)

21. (new) The method of claim 13, wherein said first layer is separated from said semiconductor substrate only by a thickness of said gate dielectric.